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10/583,844	06/22/2006	Philippe Le Roy	PF030184	6282

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EXAMINER	
PELLIGRINO, JEFFREY S	
ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/583,844	LE ROY ET AL.	
	Examiner	Art Unit	
	JEFF PELLIGRINO	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/23/2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 8, 11, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Koyama et al (U.S. Publication # 2003/0107534), hereinafter referenced as Koyama.

Regarding **claim 1**, Koyama discloses:

light emitters arranged as rows of light emitters and columns of light emitters to form an array of light emitters [figures 9 and 4],

a silicon substrate on which control means to control the emissions of the light emitters are fabricated [paragraph 0194],

the said control means including: means for powering the light emitters [power supply line 105, paragraph 0076, figure 9],

a plurality of addressing electrodes arranged according to the columns of light emitters, and intended to transmit a voltage representing an image datum to each column of light emitters [source signal line 106, paragraph 0076, figure 9],

a plurality of selection electrodes arranged according to the rows of light emitters, and intended to transmit a selection signal to each row of light emitters [a gate signal line 113, paragraph 0076, figure 9],

a plurality of modulation transistors, each associated with a light emitter of the array, the said modulation transistors including a gate electrode intended to be connected to an addressing electrode and two current-carrying electrodes, each modulation transistor intended to have a drain current pass through it to power the said light emitter for a voltage between its gate electrode and one of its current-carrying electrodes that is greater than or equal to a threshold trigger voltage, the said modulation transistors being arranged in columns associated with the columns of light emitters and being aligned on the substrate according to a guiding line [EL driving TFT 102, paragraph 0076, figures 1 and 4],

a load capacitor connected to the terminals of each modulation transistor and intended to set an electric potential at the gate electrode of the associated modulation transistor [capacitor 119, figure 9], and

a plurality of compensating transistors intended to compensate for the threshold trigger voltage of the modulation transistors by adjusting the charge on the capacitor, characterized in that wherein a single compensating transistor is connected to all the modulation transistors of a given column and is intended to compensate for the threshold trigger voltages of all the said modulation transistors of this column, and wherein the said compensating transistor is formed in the extension of the line-

arrangement of the said modulation transistors of a given column according to the said same guiding line [correction TFT 914, paragraph 0101, figure 9].

Regarding **claim 2**, Koyama discloses everything as applied above (see claim 1), in addition, Koyama discloses wherein the control means do not include any means allowing the flow of current from any one of the addressing electrodes to the means for powering the light emitters [figure 9].

Regarding **claim 3**, Koyama discloses everything as applied above (see claim 1), in addition, Koyama discloses wherein the control means include at least one voltage generator connected to one or to each addressing electrode in order to transmit a voltage representing an image datum [signal input line 107, paragraph 0081, figure 9].

Regarding **claim 4**, Koyama discloses everything as applied above (see claim 1), in addition, Koyama discloses wherein the compensating transistor of each column of light emitters includes two current-carrying electrodes, each current-carrying electrode being connected in series between the addressing electrode of this same column and the modulation transistors of this same column [correction TFT 914, figure 9].

Regarding **claim 5**, Koyama discloses everything as applied above (see claim 1), in addition, Koyama discloses wherein each compensating transistor includes a gate electrode and two current-carrying electrodes, the gate electrode of each compensating

transistor being connected to the gate electrode of all the modulation transistors of the associated column, in that one current-carrying electrode of each compensating transistor is connected to the addressing electrode of the associated column of light emitters, and in that the other current-carrying electrode of each compensating transistor is connected to its gate electrode [correction TFT 914, figure 9].

Regarding **claim 8**, Koyama discloses everything as applied above (see claim 1), in addition, Koyama discloses wherein the control means include initialization means for initializing the load capacitors intended to discharge all the load capacitors connected to the modulation transistors of a column [reset TFT 117, paragraph 0135, figure 9 and 10].

Regarding **claim 11**, Koyama discloses everything as applied above (see claim 1), in addition, Koyama discloses wherein the control means include a plurality of selection transistors having a gate electrode and two current-carrying electrodes, each selection transistor having one current-carrying electrode connected to a modulation transistor, a gate electrode connected to a selection electrode and one current-carrying electrode connected to the compensating transistor of a column of light emitters [switching TFT 111, paragraph 0076, figure 9].

Regarding **claim 13**, Koyama discloses everything as applied above (see claim 1), in addition, Koyama discloses wherein the method includes a step for applying a

voltage representing an image datum to each addressing electrode of each column of light emitters [signal input line 107, paragraph 0081, figure 9].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama in view of Hatano et al (U.S Publication # 2004/0017365), hereinafter referenced as Hatano.

Regarding **claim 6**, Koyama discloses everything claimed as applied above (see claim 1), however, Koyama fails to disclose *"wherein the said modulation transistors and the said associated compensating transistor are fabricated on a polycrystalline silicon substrate obtained by heating an amorphous silicon substrate, using a laser beam, the said beam being intended first to heat a first rectangular heating surface of the substrate, then to move in a direction of movement and then to heat a second rectangular heating surface, and in that the said modulation transistors associated with the light emitters of a given column and the associated compensating transistor are*

aligned in one and the same heating surface, the guiding alignment line extending approximately perpendicularly to the direction of movement of the laser beam."

In a similar field of endeavor, Hatano discloses wherein the said modulation transistors and the said associated compensating transistor are fabricated on a polycrystalline silicon substrate obtained by heating an amorphous silicon substrate, using a laser beam, the said beam being intended first to heat a first rectangular heating surface of the substrate, then to move in a direction of movement and then to heat a second rectangular heating surface, and in that the said modulation transistors associated with the light emitters of a given column and the associated compensating transistor are aligned in one and the same heating surface, the guiding alignment line extending approximately perpendicularly to the direction of movement of the laser beam [paragraph 0007-0008, figures 34A-B].

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Koyama by specifically providing *"wherein the said modulation transistors and the said associated compensating transistor are fabricated on a polycrystalline silicon substrate obtained by heating an amorphous silicon substrate, using a laser beam, the said beam being intended first to heat a first rectangular heating surface of the substrate, then to move in a direction of movement and then to heat a second rectangular heating surface, and in that the said modulation transistors associated with the light emitters of a given column and the associated compensating transistor are aligned in one and the same heating surface, the guiding alignment line extending approximately perpendicularly to the direction of movement of*

the laser beam", as taught by Hatano, for the purpose of improving the performance of the TFT's [Hatano, paragraph 0011-0012].

Claims 7 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama.

Regarding **claim 7**, Koyama discloses everything claimed as applied above (see claim 1), in addition, Koyama discloses wherein the said modulation transistors and the said associated compensating transistor each include a channel between two layers of doped material, the said channel being connected to their gate electrode, and in that the channel of the modulation transistors of a column and the channel of the associated compensating transistor have a main axis approximately parallel to the said guiding line [EL driving TFT 102 and correction TFT 101, figure 9].

Koyama does not disclose expressly the main axis is parallel to the guiding line (side of the substrate).

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to change the orientation of the transistors because Applicant has not disclosed that the specific orientation claimed provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with a different transistor orientation because it would not have a significant, if any, impact of the performance of the circuit.

Therefore, it would have been an obvious matter of design choice to modify Koyama to obtain the invention as specified in claim 7.

Regarding **claim 12**, Koyama disclose everything claimed as applied above (see claim 1), however, Koyama fails to disclose wherein the light emitters are organic electroluminescent diodes. The Examiner takes official notice that it would have been obvious to one of ordinary skill in that art at the time the invention was made implement the display device as taught by Koyama with organic EL elements (Koyama teach using EL elements) for the purpose of, among other reasons, improving power consumption.

Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama in view of Lo (U.S Patent # 6,937,215), hereinafter referenced as Lo.

Regarding **claim 9**, Koyama discloses everything claimed as applied above (see claim 8), in addition, Koyama discloses wherein the initialization means include an initialization transistor having a gate electrode and two current-carrying electrodes, one current-carrying electrode of the said initialization transistor being connected to the gate electrode of the modulation transistors of the said column [reset TFT 117, figure 1], however, Koyama fails to disclose *"the gate electrode of the said initialization transistor being connected to a current-carrying electrode and to the addressing electrode of a column of light emitters."*

In a similar field of endeavor, Lo discloses the gate electrode of the said initialization transistor being connected to a current-carrying electrode and to the addressing electrode of a column of light emitters [reset TFT T4, column 4, lines 55-59, figure 1].

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Koyama by specifically providing "the gate electrode of the said initialization transistor being connected to a current-carrying electrode and to the addressing electrode of a column of light emitters", as taught by Lo, for the purpose of providing a circuit for precisely compensating for the threshold voltage of the TFT's [Lo, column 3, lines 23-29].

Regarding **claim 10**, Koyama discloses everything claimed as applied above (see claim 8), however, Koyama fails to disclose *"wherein the initialization means include a diode, the cathode of which is connected to the gate electrode of the modulation transistors and the anode of which is connected to the addressing electrode of a column of light emitters."*

In a similar field of endeavor, Lo discloses wherein the initialization means include a diode, the cathode of which is connected to the gate electrode of the modulation transistors and the anode of which is connected to the addressing electrode of a column of light emitters [reset TFT T4, column 4, lines 55-59, figure 1].

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Koyama by specifically providing *"wherein the*

initialization means include a diode, the cathode of which is connected to the gate electrode of the modulation transistors and the anode of which is connected to the addressing electrode of a column of light emitters", as taught by Lo, for the purpose of providing a circuit for precisely compensating for the threshold voltage of the TFT's [Lo, column 3, lines 23-29].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEFF PELLIGRINO whose telephone number is (571)270-3572. The examiner can normally be reached on Mon.- Fri. 7:30am-5:00pm ET (alt. Fridays off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeff Pelligrino
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